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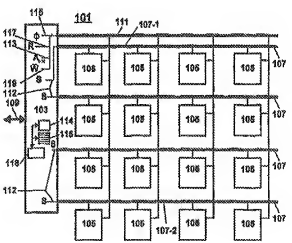

(57) Abstract

This disclosure provides a memory system and device for synchronizing response across multiple memory devices (105), whether arranged serially upon a single data bus, in parallel across multiple data busses (107), or both. A memory controller (103) periodically configures the system (101) by separately placing each memory chip (105) into a configuration mode. While in this mode, the chip (105) is polled by the controller (103) along the corresponding data bus (107), and the chip (105) responds with a reply. The controller (103) uses this reply to compute elapsed time between polling and the reply. Using all of the chips (105), the controller (103) determines the maximum response time, in terms of elapsed clock cycles. Based on this maximum time, and the individual response times for each chip, the controller (103) then programs each chip (105) with a number which defines chip-based delay (149) for responses to data read operations. In this manner, successive data reads can be performed on successive clock cycles without awaiting prior completion of earlier data reads. In addition, in a multiple data bus system, the controller (103) is not delayed by having to wait for all simultaneous data reads across a wide bus.